

The receiver chip was fabricated with a SiGe-bipolar transistor process (180 GHz transit frequency, 200 GHz maximum oscillation frequency) of Infineon Technologies. A detailed description of the circuit including its electrical characterization is given in [4]. The 1:2-DEMUX can be operated up to 100 Gbit/s at the input, resulting in 2×50 Gbit/s at the output. A minimum voltage swing of 120 mV (single ended) is needed at the input. The voltage swing at the outputs into an external 50 Ohm load is 250 mV single ended and 500 mV differential. The CDR provides recovered 50 GHz and 25 GHz clock output signals. The whole receiver chip requires a single supply voltage of -5 V and has a power dissipation of 5 W. All inputs and outputs are internally terminated with 50 Ohm. The receiver chip includes about 1000 transistors and has a size of 1.7 mm x 2.5 mm.

3 Experimental Setup

A schematic of the experimental setup comprising the 100 Gbit/s optical time division multiplexing (OTDM) transmitter, the 480 km fiber link and the 100 Gbit/s ETDM receiver is shown in Fig. 2. In the transmitter a 12.5 GHz semiconductor mode-locked pulse source (TMLL) emitted optical pulses (pulse width 1.3 ps, center wavelength 1551.5 nm) which were amplified and intensity modulated at 12.5 Gbit/s with a LiNbO_3 Mach-Zehnder modulator (Mod.). The data signal was amplified and multiplexed in an OTDM-MUX from 12.5 to 100 Gbit/s.

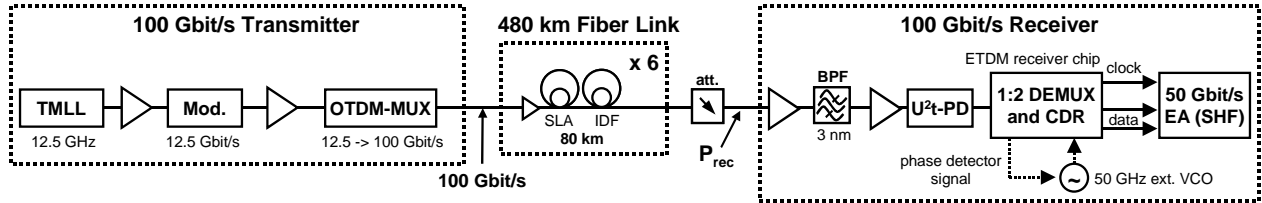


Fig. 2. Schematic depiction of the transmission experimental setup

The 100 Gbit/s data signal was transmitted over six 80 km spans of dispersion managed fiber (53 km Super Large Area fiber SLA with $D= 20$ ps/nm/km, 27 km Inverse Dispersion Fiber IDF with $D= -40$ ps/nm/km, provided by OFS Denmark). The fiber link was 100% dispersion and dispersion slope compensated. The span input power was +7 dBm. The average differential group delay of the link was 1.0 ps. In the 100 Gbit/s receiver the data signal was optically preamplified to +12 dBm average power using two erbium-doped fiber amplifiers with a 3 nm bandpass filter (BPF) in between and detected with a high-speed photodiode (PD) provided by u²t photonics. The electrical 100 Gbit/s signal was fed into the integrated ETDM receiver chip, comprising the 1:2-DEMUX and the CDR. For operation at 100 Gbit/s an external 50 GHz VCO was used with a control circuit driven by the phase-detector signal generated on the receiver chip. The demultiplexed 50 Gbit/s tributaries were detected with a 50 Gbit/s error analyzer (EA, provided by SHF) synchronized by the recovered 25 GHz clock signal from the receiver chip. An optical attenuator (att.) in conjunction with the preamplifier was used to vary the received power (P_{rec} , as indicated in Fig. 2).

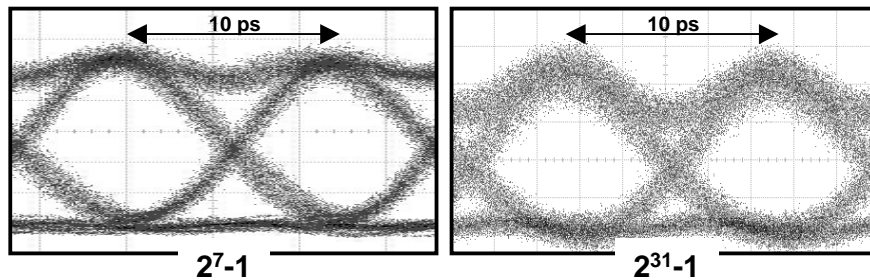


Fig. 3. 100 Gbit/s eye diagrams after the transmitter for different word lengths (Left: 508 bits, 2^7-1 at 12.5 Gbit/s base data rate; Right: $2^{31}-1$ at 50 Gbit/s base data rate).

Note that the OTDM-MUX in the transmitter was designed for standard STM-base rates and did not preserve the pseudo random bit sequence. Therefore the error analyzer was programmed to the expected bit pattern at a word length of 508 bit ($4 \times 2^7-1$). However, the delay in the OTDM-MUX was sufficient to decorrelate the data pattern. For a word length of $2^{31}-1$ a programming of the error analyzer was not possible. To address the receiver chip performance at longer word length a slightly different transmitter setup was used. This transmitter was operated at a base data rate of 50 Gbit/s instead of 12.5 Gbit/s and comprised a modulation at 50 Gbit/s with subsequent optical multiplexing to 100 Gbit/s. As shown in Fig. 3 this transmitter produced a significantly degraded data signal and was therefore only used in back-to-back measurements.

